TITLE OF THE INVENTION

POWER MOS TRANSISTOR HAVING TRENCH GATE

CROSS-REFERENCE TO RELATED APPLICATIONS

PC 2/15/07

This application is a continuation of U.S. patent application 09/667,559 filed 09/22/2000, abandoned, which claims benefit of priority under 35 U.S.C. 119 to Japanese Patent Application No. P11-269922 filed September 24, 1999, the entire contents of which are incorporated by reference herein.

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a structure of a power MOS transistor having a trench gate.

Discussion of the Background

Fig. 1 is a plan view showing a spline-structured MOS transistor manufactured based on current product design rules. Trench gates 45 and source contacts 46 are alternately formed on a semiconductor substrate. Each of the source contacts 46 is connected to a source electrode formed on a layer formed further thereon.

Fig. 2 is an upper surface view showing a pattern of an offset mesh-structured MOS transistor manufactured based on current product design rules. Trench gates 38 and source contacts 44 are alternately formed on a semiconductor substrate. Each of the source contacts 44 is connected to a source electrode formed on a layer formed further thereon. The offset mesh type is designed to realize a high degree of integration by